COMMUNICATIONS IN COMPUTATIONAL PHYSICS
Vol. **3**, No. 2, pp. 376-396

Commun. Comput. Phys.
February 2008

RLC Equivalent Circuit Synthesis Method for Structure-Preserved Reduced-Order Model of Interconnect in VLSI

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Received 12 February 2007; Accepted (in revised version) 25 July 2007

Communicated by Wei Cai

Available online 8 October 2007

Abstract. This paper aims to explore RLC equivalent circuit synthesis method for reduced-order models of interconnect circuits obtained by Krylov subspace based model order reduction (MOR) methods. To guarantee pure RLC equivalent circuits can be synthesized, both the structures of input and output incidence matrices and the block structure of the circuit matrices should be preserved in the reduced-order models. Block structure preserving MOR methods have been well established. In this paper, we propose an embeddable *I*nput-*O*utput structure *P*reserving *O*rder *R*eduction (IOPOR) technique to further preserve the structures of input and output incidence matrices. By combining block structure preserving MOR methods and IOPOR technique, we develop an RLC equivalent circuit synthesis method *RLCSYN* (RLC SYNthesis). Inline diagonalization and regularization techniques are specifically proposed to enhance the robustness of inductance synthesis. The pure RLC model, high modeling accuracy, passivity guaranteed property and SPICE simulation robustness make *RLCSYN* more applicable in interconnect analysis, either for digital IC design or mixed signal IC simulation.

AMS subject classifications: 94C05, 93A15, 68U07, 68U20, 41A21

Key words: Interconnect circuit, model order reduction, equivalent circuit synthesis.

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1 Introduction

In modern high-speed nano-scale ULSI design, interconnects have become a dominant factor in determining the performance of the whole chip. However, the extracted interconnect circuits, either based on RLC or RCS model, turn out to be extremely large, which poses great challenges to interconnect analysis techniques [1, 2].

Model order reduction (MOR) has become the state-of-the-art technique for fast simulation of the interconnect circuits with large dimensions. Recently, RLC-in-RLC-out MOR has become a research intensive area [3–7]. In a typical design flow, all kinds of circuit analysis and verification procedures, such as static timing analysis, dynamic simulation, noise analysis, circuit checking and power analysis, take extracted RLC circuits as inputs. If RLC equivalent circuit of the reduced-order models is not available, all the downstream circuit simulators and associated programs have to be modified to handle transfer functions or state-space models of interconnects [8]. RLC equivalent circuit also plays an important role in mixed signal IC simulation, where linear and nonlinear circuits need to be simulated together. Moreover, some analysis tools such as circuit checker only accept RLC circuits as inputs [3].

Realizable reduction methods providing RLC-in-RLC-out (RC-in-RC-out) reduction schemes are proposed in [3–5]. Since these reduction methods are based on selectively removing non-terminal nodes by Guassian elimination, the applications of these methods would be limited. In [3, 5], only the nodes satisfying strict nodal time constant constraints can be eliminated. These constraints would limit the circuit reduction ratio, which makes [3, 5] serve as a preprocessing step before feeding extracted circuits to moment-matching based MOR methods [3]. In [4], although high reduction ratio is achievable, high order approximation of admittances induced by elimination should be calculated and substituted in each elimination to guarantee accuracy of the reduced-order circuit model, which would be computation intensive.

Krylov subspace based MOR methods are the state-of-the-art techniques for interconnect analysis. Compared with realizable reduction methods, Krylov subspace based MOR methods can achieve higher reduction ratio and accuracy [9]. However, RLC equivalent circuit synthesis method for Krylov subspace based MOR methods has not been well established. In [10], Freund et al. proposed an equivalent RC circuit synthesis method for single-port RC reduced-order models derived from SyPVL method. Equivalent circuit synthesis techniques for reduced-order models of multi-port RLC circuits obtained by PRIMA(-like) algorithm(s) are well investigated in [7]. However, since the input-output and block structures are not preserved in PRIMA(-like) algorithm(s), controlled sources should be introduced in the synthesized circuits in these methods. Up to now, pure RLC equivalent circuits are not achievable yet.

In this paper, we propose an RLC equivalent circuit synthesis method for reduced-order model obtained by Krylov subspace based MOR methods. For the synthesis of pure RLC models, both the structures of input and output incidence matrices and the block structures of the circuit matrices should be preserved. We employ SPRIM [11] or

SAPOR [12] to preserve the block structure and further propose an embeddable *I*nput-*O*utput structure *P*reserving *O*rder *R*eduction (IOPOR) technique to preserve the structures of input and output incidence matrices. As a result, we develop an RLC equivalent circuit synthesis method (*RLCSYN* in short), by combining block structure preserving MOR methods and IOPOR technique. Inline diagonalization and regularization techniques are also specifically derived to enhance the robustness of inductance synthesis. The synthesized circuit by *RLCSYN* method presents merits as pure RLC model, high accuracy, passivity preserving and SPICE simulation robustness, which makes *RLCSYN* more applicable in practical interconnect analysis.

The remainder of the paper is organized as follows. In Section 2, we review the block structure preserving MOR methods. The embeddable IOPOR method and circuit synthesis procedure are proposed in Sections 3 and 4 respectively. Numerical experiments are demonstrated in Section 5. In Section 6, we conclude the paper.

2 Background

The block structure preserving MOR methods SPRIM [11] and SAPOR [12] are briefly reviewed in this section.

2.1 SPRIM

For a p-input q-output RLC interconnect network, the time-domain MNA circuit equations can be described as

$$\begin{cases} \begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix} \begin{bmatrix} \dot{v}(t) \\ \dot{i}(t) \end{bmatrix} + \begin{bmatrix} G & E \\ -E^T & 0 \end{bmatrix} \begin{bmatrix} v(t) \\ i(t) \end{bmatrix} = \begin{bmatrix} B_v u(t) \\ 0 \end{bmatrix}, \\ y(t) = D_v^T v(t), \end{cases} \tag{2.1}$$

where $v(t) \in R^N$ and $i(t) \in R^M$ denote N nodal voltages and the M auxiliary branch currents, respectively, $u(t) \in R^p$ and $y(t) \in R^q$ are the input current sources and output voltages, $B_v \in R^{N\times p}$ and $D_v \in R^{N\times q}$ denote the incidence matrices for the input current sources and output node voltages, $C \in R^{N\times N}$, $L \in R^{M\times M}$ and $G \in R^{N\times N}$ represent the contributions of the capacitors, inductors and resistors, respectively, $E \in R^{N\times M}$ is the incidence matrix for the inductances.

Performing the Laplace transform for Eq. (2.1), we have the MNA circuit equations in frequency domain

$$\begin{cases} \left(s \begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix} + \begin{bmatrix} G & E \\ -E^T & 0 \end{bmatrix} \right) \begin{bmatrix} v(s) \\ i(s) \end{bmatrix} = \begin{bmatrix} B_v u(s) \\ 0 \end{bmatrix}, \\ y(s) = D_v^T v(s), \end{cases} \tag{2.2}$$

where $v(s)$, $i(s)$, $u(s)$ and $y(s)$ are Laplace transforms of $v(t)$, $i(t)$, $u(t)$ and $y(t)$, respectively.

A block structure-preserving technique SPRIM was proposed in [11]. SPRIM employs the well-known block Arnoldi algorithm to construct an orthonormal basis $V\in R^{(N+M)\times n}$ of Krylov subspace spanned by the first k block moments of the state variables in (2.2). Instead of directly using $V=[V_1\ \ V_2]^T$ as the projection matrix, a larger orthogonal matrix $\begin{bmatrix} V_1 & 0 \\ 0 & V_2 \end{bmatrix}$ is employed to project the original system (2.2) to

$$\begin{cases} \left(s\begin{bmatrix} \tilde{C} & 0 \\ 0 & \tilde{L} \end{bmatrix}+\begin{bmatrix} \tilde{G} & \tilde{E} \\ -\tilde{E}^T & 0 \end{bmatrix}\right)\begin{bmatrix} \tilde{v}(s) \\ \tilde{i}(s) \end{bmatrix}=\begin{bmatrix} \tilde{B}_v u(s) \\ 0 \end{bmatrix}, \\ y(s)=\tilde{D}_v^T\tilde{v}(s), \end{cases} \tag{2.3}$$

where

$$\tilde{C}=V_1^TCV_1,\quad \tilde{L}=V_2^TLV_2,\quad \tilde{G}=V_1^TGV_1,\quad \tilde{E}=V_2^TEV_1,\quad \tilde{B}_v=V_1^TB_v,\quad \tilde{D}_v=V_1^TD_v.$$

Here, $V_1\in R^{N\times n}$, $V_2\in R^{M\times n}$.

By eliminating the auxiliary variables $\tilde{i}(s)$, a second-order formulation of the reduced system (2.3) of order n is given by

$$\begin{cases} \left(s\tilde{C}+\tilde{G}+\frac{1}{s}\tilde{E}\tilde{L}^{-1}\tilde{E}^T\right)\tilde{v}(s)=\tilde{B}_v u(s), \\ y(s)=\tilde{D}_v\tilde{v}(s). \end{cases} \tag{2.4}$$

It is obvious that the reduced system (2.3) exactly preserves the block structure of the original system (2.2).

2.2 SAPOR

Since the susceptance matrix can be viewed as the inverse of inductance matrix, the MNA equation for RCS circuit in frequency domain can be expressed as

$$\begin{cases} \left(s\begin{bmatrix} C & 0 \\ 0 & I \end{bmatrix}+\begin{bmatrix} G & E \\ -SE^T & 0 \end{bmatrix}\right)\begin{bmatrix} v(s) \\ i(s) \end{bmatrix}=\begin{bmatrix} B_v u(s) \\ 0 \end{bmatrix}, \\ y(s)=D_v^Tv(s), \end{cases} \tag{2.5}$$

where S represents the susceptance matrix and $S=L^{-1}$.

The RCS interconnect circuits are more preferred to be formulated in a second-order form in frequency-domain

$$\begin{cases} (sC+G+\frac{1}{s}\Gamma)v(s)=B_v u(s), \\ y(s)=D_v^Tv(s), \end{cases} \tag{2.6}$$

where $\Gamma=ESE^T$, and $\Gamma\in R^{N\times N}$, since all the system matrices C, G and Γ are symmetric and positive semi-definite in the second-order form.

In [12, 13], a numerically stable procedure is proposed to generate an orthonormal basis $Q \in R^{N\times n}$ of the block Krylov subspace spanned by the first k block moments of the node voltages variables $v(s)$ in (2.6). Afterwards, a Q-based orthogonal projection is performed on the original system (2.6) to obtain the reduced-order model of order n

$$\begin{cases} (s\tilde{C}+\tilde{G}+\frac{1}{s}\tilde{\Gamma})\tilde{v}(s)=\tilde{B}_v u(s), \\ y(s)=\tilde{D}_v^T\tilde{v}(s), \end{cases} \tag{2.7}$$

where

$$\tilde{C}=Q^TCQ, \quad \tilde{G}=Q^TGQ, \quad \tilde{\Gamma}=Q^T\Gamma Q, \quad \tilde{B}_v=Q^TB_v, \quad \tilde{D}_v=Q^TD_v.$$

Obviously, the reduced-order model (2.7) exactly preserves the block structure of the original system (2.6).

2.3 Limitations

The structure preserving property facilitates synthesizing actual RLC circuits from the reduced-order models. However, since the structures of input and output incidence matrices are not preserved, controlled sources should be introduced in the synthesized circuits. For example, for each row of the matrix B_v in the original system (2.2) or (2.6), at most one entry is 1 and all others are zeros, since each input current sources is attached to one specified internal node as an excitation. Nevertheless, in the reduced current sources incidence matrix $\tilde{B}_v$, multiple nonzero entries with different values exist in each row. This means multiple input current sources are combined together to add an excitation to each internal node. In order to characterize this kind of excitation property, controlled sources should be introduced. Similarly, controlled sources should be introduced to model the output property induced by dense property of $\tilde{D}_v$.

In the next section, we propose a technique to enhance SPRIM and SAPOR such that both block structure and the structures of input and output incidence matrices can be preserved in the reduced-order models.

3 IOPOR: Input-Output structure Preserving Order Reduction technique

In the rest of the paper, we only discuss IOPOR and RLC equivalent circuit synthesis method for SAPOR [12]. Following the same principle, IOPOR technique and RLC equivalent circuit synthesis method can be easily derived for SPRIM [11].

In order to preserve the structures of input and output incidence matrices of system (2.6) in its reduced-order model (2.7), the MNA equation for RCS circuit is reformulated as

$$\begin{cases} \left(s\begin{bmatrix} C_x & 0 \\ 0 & I \end{bmatrix}+\begin{bmatrix} G_x & E_x \\ -S_xE_x^T & 0 \end{bmatrix}\right)\begin{bmatrix} v_x(s) \\ i_x(s) \end{bmatrix}=\begin{bmatrix} B_x \\ 0 \end{bmatrix}u(s), \\ y(s)=D_x^Tv_x(s), \end{cases} \tag{3.1}$$

where the first p rows of circuit equations represent the p Kirchhoff Current Law (KCL) formulated at p input nodes and the $(p+1)$-th to $(p+q)$-th rows represent the q KCL equations formulated at q output nodes. Here, we assume input and output nodes are different[†]. The nonzero entries which relate current sources to input nodes or map inner nodes to output nodes, are now concentrated in the first $p+q$ rows of B_x and D_x in (3.1). In the following, we denote $r=p+q$ the total number of input and output nodes. As a result, in (3.1),

$$B_x=\left[\begin{array}{cc} B_{v1}^T & 0 \end{array}\right]^T\in R^{N\times p},\quad D_x=\left[\begin{array}{cc} D_{v1}^T & 0 \end{array}\right]^T\in R^{N\times q}.$$

Here, $B_{v1}\in R^{r\times p}$ and $D_{v1}\in R^{r\times q}$. In fact, the system (3.1) can also be regarded as a permuted system of (2.5).

By eliminating $i_x(s)$ in (3.1), we have the reformulated second-order system

$$\left\{\begin{array}{l} (sC_x+G_x+\frac{1}{s}\Gamma_x)v_x(s)=B_xu(s),\\ y(s)=D_x^Tv_x(s), \end{array}\right. \tag{3.2}$$

where $\Gamma_x=E_xS_xE_x^T$ and $\Gamma_x\in R^{N\times N}$.

According to the block structures of $\left[\begin{array}{cc} B_{v1}^T & 0 \end{array}\right]^T$ and $\left[\begin{array}{cc} D_{v1}^T & 0 \end{array}\right]^T$, the projection matrix $Q_x\in R^{N\times n}$ of Eq. (3.2) generated by SAPOR [12, 13] is partitioned into two parts

$$Q_x=\left[\begin{array}{c} Q_{x1}\\ Q_{x2} \end{array}\right], \tag{3.3}$$

where $Q_{x1}\in R^{r\times n}$ has the same number of rows as that of B_{v1} and $Q_{x2}\in R^{(N-r)\times n}$. We construct a new projection matrix W based on Q_x as following

$$W=\left[\begin{array}{cc} I_{r\times r} & 0\\ 0 & Q_{x2} \end{array}\right], \tag{3.4}$$

where $I_{r\times r}$ is an $r\times r$ identity matrix and $W\in R^{N\times(n+r)}$.

With the projection matrix W, the reduced-order model of (3.2) is constructed as

$$\left\{\begin{array}{l} (s\tilde{C}_x+\tilde{G}_x+\frac{1}{s}\tilde{\Gamma}_x)\tilde{v}_x(s)=\tilde{B}_xu(s),\\ y(s)=\tilde{D}_x^T\tilde{v}_x(s), \end{array}\right. \tag{3.5}$$

where

$$\begin{aligned} &\tilde{C}_x=W^TC_xW,\quad \tilde{G}_x=W^TG_xW,\quad \tilde{\Gamma}_x=W^T\Gamma_xW,\\ &\tilde{B}_x=W^TB_x=\left[\begin{array}{cc} B_{v1}^T & 0_{p\times n} \end{array}\right]^T,\quad \tilde{D}_x=W^TD_x=\left[\begin{array}{cc} D_{v1}^T & 0_{q\times n} \end{array}\right]^T. \end{aligned}$$

Here, $0_{p\times n}$ and $0_{q\times n}$ denote $p\times n$ and $q\times n$ dimensional zero matrices, respectively. The input output structure B_{v1} and D_{v1} are preserved in the reduced-order system (3.5). Compared with the reduced order model (2.7), the order of (3.5) is $n+r$ rather than n. In the rest of the paper, we denote m the number of reduced order of (3.5).

[†]It can be tackled similarly when input and output nodes are overlapping.

The proposed embeddable IOPOR method has the following properties:

Moment matching: For projection matrix W, we have $colspan\{Q_x\} \subseteq colspan\{W\}$. The reduced-order model (3.5) obtained by IOPOR, i.e., projecting original system (3.2) onto W matches at least as many moments as the reduced-order model obtained by SAPOR, i.e., projecting original system (3.2) onto Q_x [14].

Input and output structure preserving: The input and output structures B_{v1} and D_{v1} in incidence matrices B_x and D_x in (3.2) are exactly preserved in the reduced-order model (3.5).

4 RLCSYN: RLC equivalent circuit synthesis

By combining IOPOR with the block structure preserving MOR methods such as SPRIM [11] and SAPOR [12], both the block structure and input and output structures can be preserved. Therefore, pure RLC equivalent circuit can be synthesized. In this section, we propose the RLC equivalent circuit synthesis method RLCSYN for reduced-order model (3.5). Inline diagonalization and regularization techniques are also specifically derived to enhance the robustness of inductance synthesis.

4.1 RLC circuit synthesis by unstamping procedure

Actually, the second-order formula (3.5) can be viewed as the nodal equation of a circuit with m nodes, which describes the Kirchhoff Current Law (KCL) satisfied in each node of the circuit. Correspondingly, the matrices $s\tilde{C}_x$, $\tilde{G}_x$ and $\tilde{\Gamma}_x/s$ denote the node-admittance matrices of the capacitors, the resistors and the susceptances, respectively. $\tilde{B}_x$ represents the incidence matrix of input current sources to internal nodes. $\tilde{D}_x$ represents the incidence matrix of inner nodes to output nodes. Based on these observations, the equivalent circuit synthesis procedure from the second-order formula (3.5) is actually an inverse procedure of constructing the nodal equation by stamping.

Assume the m nodes in the equivalent circuit are $n_1,n_2,\cdots,n_m$, and the corresponding nodal voltages are $v_1,v_2,\cdots,v_m$, respectively. Denote $\tilde{c}_{ij}$, $\tilde{g}_{ij}$, $\tilde{\delta}_{ij}$, $\tilde{b}_{ij}$ and $\tilde{d}_{ij}$ the elements in the i-th row and j-th column of $\tilde{C}_x$, $\tilde{G}_x$, $\tilde{\Gamma}_x$, $\tilde{B}_x$ and $\tilde{D}_x$ respectively. We can construct the equivalent circuit of (3.5) in the following unstamping procedure.

Step 1. Construct resistance network by examining the resistance node-admittance matrix $\tilde{G}_x$.

In Fig. 1, we show the constructed resistance network for node n_i. According to nodal equation formulation approach [1], if a resistor r_{ij} exists between node n_i and node n_j, its contributions to the (i,i) and (j,j) elements of circuit node admittance matrix is r_{ij}^{-1}. Its contributions to the (i,j) and (j,i) elements of circuit node admittance matrix is $-r_{ij}^{-1}$. If a resistor r_{ii} exists between node n_i and the ground, its contribution to the (i,i) entry in the circuit node-admittance matrix is r_{ij}^{-1}.

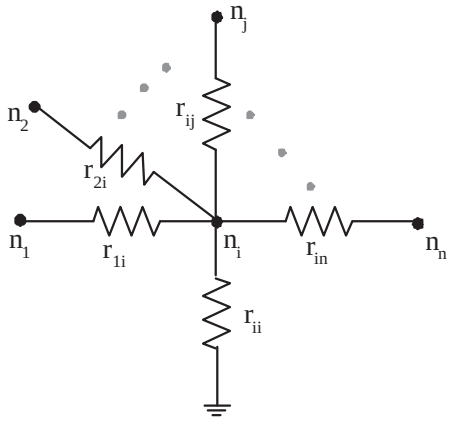

Figure 1: The resistance network of node n_i.

Therefore, in matrix $\tilde{G}_x$, the off-diagonal entry $\tilde{g}_{ij}$ is only contributed by the resistor existing between nodes n_i and n_j, but the diagonal entry $\tilde{g}_{ii}$ is contributed by all the resistors connected to node n_i from the ground and the other nodes $n_1, n_2, \cdots, n_j, \cdots, n_m$ ($j \neq i$). Based on this observation, we can construct the resistance network as follows.

a). For each off-diagonal entry $\tilde{g}_{ij}$ in the upper-diagonal part of matrix $\tilde{G}_x$, if $\tilde{g}_{ij} \neq 0$, we add a resistor $r_{ij} = -\tilde{g}_{ij}^{-1}$ between n_i and n_j.

b). For each diagonal entry $\tilde{g}_{ii}$ in the matrix $\tilde{G}$, we can rewrite it as

$$\tilde{g}_{ii} = (\tilde{g}_{ii} + \tilde{g}_{i1} + \cdots \tilde{g}_{ij} + \cdots \tilde{g}_{im}) - \tilde{g}_{i1} - \cdots \tilde{g}_{ij} - \cdots \tilde{g}_{im} \quad (j \neq i),$$

where $-\tilde{g_{ij}}$ $(j \neq i)$ corresponds to the contribution of the existing resistor r_{ij} between node n_i and n_j generated in step 1(a). Therefore, we add a node-to-ground resistor r_{ii} at node n_i, whose value equals to $1/(\tilde{g}_{i1} + \tilde{g}_{i2} + \cdots + \tilde{g}_{im})$.

Step 2. Construct capacitance and inductance network by examining the capacitance node-admittance matrix $s\tilde{C}_x$ and the susceptance node admittance matrix $\tilde{\Gamma}/s$.

We can construct capacitance and inductance network similar to resistance network.

a). For each off-diagonal entry $\tilde{c}_{ij}$ in the upper-diagonal part of matrix $\tilde{C}_x$, if $\tilde{c}_{ij} \neq 0$, we add a capacitor $c_{ij} = -\tilde{c}_{ij}$ between n_i and n_j. For each off-diagonal entry $\tilde{\delta}_{ij}$ in the upper-diagonal part of matrix $\tilde{\Gamma}_x$, if $\tilde{\delta}_{ij} \neq 0$, we add an inductor $l_{ij} = \tilde{\delta}_{ij}^{-1}$ between n_i and n_j.

b). For each diagonal entry c_{ii} in the matrix $\tilde{C}_x$, we add a node-to-ground capacitor

$$c_{ii} = \tilde{c}_{i1} + \tilde{c}_{i2} + \cdots + \tilde{c}_{im}$$

at node n_i. For each diagonal entry $\tilde{\delta}_{ii}$ in the matrix $\tilde{\Gamma}_x$, we add a node-to-ground inductor $l_{ii} = 1/(\tilde{\delta}_{i1} + \tilde{\delta}_{i2} + \cdots + \tilde{\delta}_{im})$ at node n_i.

Step 3. For each non-zero entry (i.e., -1,1) $\tilde{b}_{ij}$ in $\tilde{B}_x$, connect the j-th current source to the n_i node.

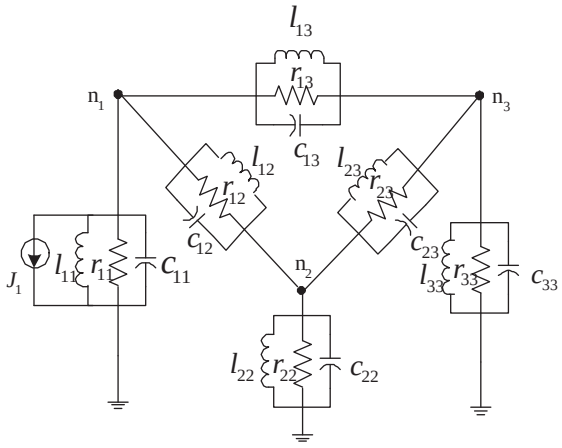

Figure 2: A sample circuit with 3 nodes synthesized by unstamping.

Step 4. For each non-zero entry (i.e., -1,1) $\tilde{d}_{ij}$ in $\tilde{D}_x$, set node n_i as the j-th output node.

4.2 Diagonalization technique

In Fig. 2, we show a sample circuit with 3 nodes synthesized by the unstamping procedure. Due to the dense property of the matrix $\tilde{\Gamma}_x$, inductor loop may occur in the synthesized circuit, as shown in Fig. 2. Because SPICE-based simulators always assume all the inductor components short-circuit for OP analysis, the existence of inductor loop will induce a short-circuit loop, and hence stop the SPICE simulation. On the other hand, due to the singularity of $\tilde{\Gamma}_x$, we cannot get the inverse of $\tilde{\Gamma}_x$ in (3.5) i.e. inductance matrix, and synthesize it as self inductors and mutual inductors to avoid inductor loops.

In this subsection, we will propose a diagonalization technique to avoid the occurrence of inductor loop in the synthesized circuit. We propose to transform the susceptance matrix $\tilde{\Gamma}_x$ into a diagonal matrix. The diagonal property guarantees only node-to-ground inductance components exist in the synthesized circuits. In the following we explain the diagonalization technique.

Considering the reduced-order model (3.5), we perform the Schur decomposition of $\tilde{\Gamma}_x$ by taking advantage of the symmetry property of $\tilde{\Gamma}_x$

$$\tilde{\Gamma}_x = \hat{U}\hat{\Gamma}_x\hat{U}^T, \tag{4.1}$$

where $\hat{\Gamma}_x \in R^{m\times m}$ is a diagonal matrix, and $\hat{U} \in R^{m\times m}$ is orthogonal.

Applying $\hat{U}$-based congruence transformation on (3.5), we get

$$\begin{cases} (s\hat{C}_x + \hat{G}_x + \frac{1}{s}\hat{\Gamma}_x)\hat{v}_x(s) = \hat{B}_x u(s), \\ y = \hat{D}_x^T \hat{v}_x(s), \end{cases} \tag{4.2}$$

where

$$\hat{C}_x = \hat{U}^T\tilde{C}_x\hat{U}, \quad \hat{G}_x = \hat{U}^T\tilde{G}_x\hat{U}, \quad \hat{B}_x = \hat{U}^T\tilde{B}_x, \quad \hat{D}_x = \hat{U}^T\tilde{D}_x.$$

Although the dense matrix $\tilde{\Gamma}_x$ is diagonalized in (4.2), the input and output structure preserved property in $\tilde{B}_x$ and $\tilde{D}_x$ in (3.5) by IOPOR technique is destroyed in $\hat{B}_x$ and $\hat{D}_x$ after this diagonalization.

To fix this problem, we propose an input-output structure preserving diagonalization method as stated in the following theorem.

Theorem 4.1. *If the original RCS circuit has no susceptances directly connected to input and output nodes, then a congruence transform matrix*

$$\bar{U}=\begin{bmatrix} I_{r\times r} & 0 \\ 0 & \bar{U}_l \end{bmatrix},$$

where $\bar{U}_l \in R^{n\times n}$, can be constructed to simultaneously guarantee the $\tilde{\Gamma}_x$ in (3.5) *being diagonalized and the structures of the input and output incidence matrices $\tilde{B}_x$ and $\tilde{D}_x$ in* (3.5) *being preserved.*

Proof. If no susceptances are directly connected to input and output nodes, the first r rows of E_x in the system (3.1) are all zeros, i.e.,

$$E_x=\begin{bmatrix} 0_{r\times M} \\ E_{x1} \end{bmatrix}, \tag{4.3}$$

where $0_{r\times M}$ represents $r\times M$ dimensional zero matrix and $E_{x1}\in R^{(N-r)\times M}$ denotes the lower part of E_x. By substituting E_x in (4.3) into $\Gamma_x = E_x S_x E_x^T$, Γ_x in the system (3.2) has the structure as

$$\Gamma_x=\begin{bmatrix} 0_{r\times r} & 0 \\ 0 & \Gamma_l \end{bmatrix}, \tag{4.4}$$

where $\Gamma_x \in R^{N\times N}$, $0_{r\times r}$ represents an $r\times r$ dimensional zero matrix and $\Gamma_l \in R^{(N-r)\times(N-r)}$ is the corresponding right-bottom part of Γ_x. Subsequently, it can be further verified that $\tilde{\Gamma}_x = W^T\Gamma_x W$ in the reduced order system (3.5) has the following structure

$$\tilde{\Gamma}_x=\begin{bmatrix} 0_{r\times r} & 0 \\ 0 & \tilde{\Gamma}_l \end{bmatrix}, \tag{4.5}$$

where $\tilde{\Gamma}_x \in R^{(n+r)\times(n+r)}$, $0_{r\times r}$ represents an $r\times r$ dimensional zero matrix and $\tilde{\Gamma}_l \in R^{n\times n}$ is the corresponding right-bottom part of $\tilde{\Gamma}_x$. Instead of performing Schur decomposition of $\tilde{\Gamma}_x$, we perform Schur decomposition of $\tilde{\Gamma}_l$,

$$\tilde{\Gamma}_l = \bar{U}_l\bar{\Gamma}_l\bar{U}_l^T, \tag{4.6}$$

where $\bar{\Gamma}_l \in R^{n\times n}$ is a diagonal matrix, and $\bar{U}_l \in R^{n\times n}$ is orthogonal.

The matrix for congruence transform is constructed as

$$\bar{U}=\begin{bmatrix} I_{r\times r} & 0 \\ 0 & \bar{U}_l \end{bmatrix}. \tag{4.7}$$

Applying $\bar{U}$-based congruent transform on (3.5), we have

$$\begin{cases} (s\bar{C}_x+\bar{G}_x+\frac{1}{s}\bar{\Gamma}_x)\bar{v}_x(s)=\bar{B}_x u(s), \\ y(s)=\bar{D}_x^T\bar{v}_x(s), \end{cases} \tag{4.8}$$

where

$$\bar{C}_x=\bar{U}^T\tilde{C}_x\bar{U},\quad \bar{G}_x=\bar{U}^T\tilde{G}_x\bar{U},\quad \bar{B}_x=\bar{U}^T\tilde{B}_x=\tilde{B}_x,\quad \bar{D}_x=\bar{U}^T\tilde{D}_x=\tilde{D}_x$$

and

$$\bar{\Gamma}_x=\begin{bmatrix} 0_{r\times r} & 0 \\ 0 & \bar{\Gamma}_l \end{bmatrix}.$$

Obviously, $\bar{\Gamma}_x$ is diagonal and the input and output incidence structures are preserved in $\bar{B}_x$ and $\bar{D}_x$. □

Similar results can also be derived for SPRIM based circuit synthesis method if the RLC circuit has no inductors directly connected to input and output nodes.

For interconnect circuits, the assumption that no susceptances (or inductors) are directly connected to input and output nodes is mostly satisfied. An interconnect circuit can be modeled as an RLC circuit model as described in (2.2), or equivalently be modeled as an RCS circuit model as described in (2.5). Susceptances and inductors share the same incidence matrix as shown in (2.5) and (2.2), which indicates they hold the same topology in RLC and RCS models. As a result, no susceptances being directly connected to input and output nodes in RCS interconnect model is equivalent to no inductors being directly connected to input and output nodes in RLC interconnect model. In RLC models of interconnects, each inductor is accompanied by a resistor. An inductor plus a resistor can be taken as an individual element. Therefore, as shown in Fig. 3, we can eliminate the cases that an inductor is directly connected to an input or output node by swapping the positions of that inductor and its corresponding resistance element while the input-output transfer characterizations of the interconnect circuit have no change.

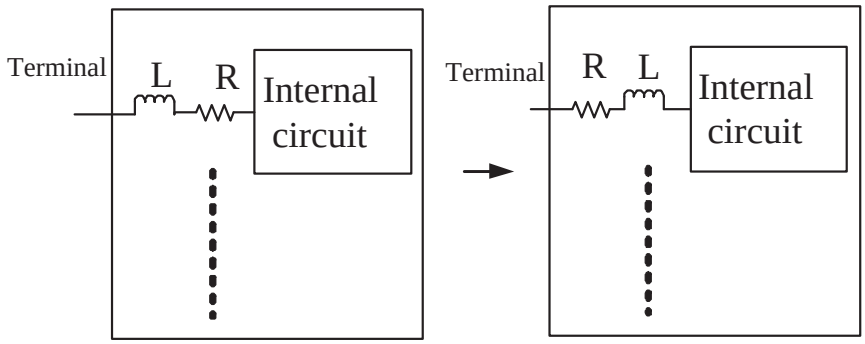

Figure 3: Swapping the positions of R and L elements doesn't change the input-output transfer characterization of the interconnect circuit.

After the diagonalization, we can easily synthesize a circuit without inductor loop based on the new reduced order equation (4.8). The construction procedure is similar as

before, except for the inductance network synthesis in Step 2, since now we can construct inductance network simply according to the diagonal matrix $\bar{\Gamma}_x$ in (4.8). The revised inductance network synthesis procedure can be described as below:

Revised Inductance Network Synthesis Procedure: For each entry $\bar{\delta}_{ii}$ in diagonal matrix $\bar{\Gamma}_x$, we add a node-to-ground inductor $l_{ii}=\bar{\delta}_{ii}^{-1}$ at node n_i.

4.3 Regularization technique

Note that the eigenvalue of $\tilde{\Gamma}_l$ i.e. diagonal entries of $\bar{\Gamma}_l$ may have very large difference in magnitude. In our numerical experiments, we found that the maximum and minimum eigenvalues of $\tilde{\Gamma}_l$ are around $\mathcal{O}(10^{10})$ and $\mathcal{O}(10^{-7})$ respectively. Correspondingly, the synthesized inductors will be 100 *ph* (*picohenry*) and 10^7 *henry*. The largest inductor 10^7 *henry* is not physically reasonable. Unfortunately these overlarge inductors may cause convergence difficulty in SPICE simulation as to be described in Section 5. From numerical computation point of view, the entries with nearly zero value in matrix $\bar{\Gamma}_l$ can be neglected while the system property is not significantly changed.

In the following, we will develop a regularization technique to get rid of the smallest entries of $\bar{\Gamma}_l$ to avoid unreasonable overlarge inductors in the synthesized circuit. We also provide an error analysis scheme to guarantee that the regularization of circuit equation is error controllable. We found that, after regularization, the synthesized circuit will be very robust to immune the convergence problem in SPICE simulation.

4.3.1 Regularization

We perform regularization on the diagonal matrix $\bar{\Gamma}_x$ in (4.8) by neglecting the smallest entries in $\bar{\Gamma}_l$. First, a threshold *tol* is chosen according to the accuracy requirement, then $\bar{\Gamma}_l$ is reordered into

$$\bar{\Gamma}_l=\begin{bmatrix} \bar{\Gamma}_{l1} & 0 \\ 0 & \bar{\Gamma}_{l2} \end{bmatrix}, \tag{4.9}$$

where all the entries in $\bar{\Gamma}_{l1}$ is larger than $tol\cdot\|\bar{\Gamma}_x\|$, whereas the entries in $\bar{\Gamma}_{l2}$ is less than $tol\cdot\|\bar{\Gamma}_x\|$. Correspondingly, $\bar{\Gamma}_x$ becomes

$$\bar{\Gamma}_x=\begin{bmatrix} 0 & 0 & 0 \\ 0 & \bar{\Gamma}_{l1} & 0 \\ 0 & 0 & \bar{\Gamma}_{l2} \end{bmatrix}. \tag{4.10}$$

Afterwards, $\bar{\Gamma}_{l2}$ is neglected, and $\bar{\Gamma}_x$ is regularized into

$$\bar{\tilde{\Gamma}}_x=\begin{bmatrix} 0 & 0 & 0 \\ 0 & \bar{\Gamma}_{l1} & 0 \\ 0 & 0 & 0 \end{bmatrix}. \tag{4.11}$$

The criterion of regularization can be described as

$$\left\|\bar{\Gamma}_x-\bar{\tilde{\Gamma}}_x\right\|\leq tol\cdot\|\bar{\Gamma}_x\|. \tag{4.12}$$

The diagonalized circuit equation (4.8) becomes

$$\begin{cases} (s\bar{C}_x+\bar{G}_x+\frac{1}{s}\bar{\bar{\Gamma}}_x)\bar{\bar{v}}_x(s)=\bar{B}_x u(s), \\ y(s)=\bar{D}_x^T\bar{\bar{v}}_x(s). \end{cases} \tag{4.13}$$

From the viewpoint of circuit synthesis, the regularization of $\bar{\Gamma}_x$ is equivalent to the elimination of the overlarge inductors in the synthesized circuit. According to the electrical property of the inductance, the overlarge inductor will cause the corresponding branch almost open. Therefore, the neglect of the overlarge inductors will bring in trivial influence on the circuit response, but facilitate the convergence of SPICE simulation. Furthermore, the error induced by the regularization is controllable, as shown in the following error analysis.

4.3.2 Error analysis

Denote $\bar{A}=\bar{G}_x+s\bar{C}_x+\frac{1}{s}\bar{\Gamma}_x$, $\delta\bar{A}=\frac{1}{s}(\bar{\bar{\Gamma}}_x-\bar{\Gamma}_x)$. The solution of $\bar{v}_x(s)$ in (4.8) can be expressed as

$$\bar{v}_x(s)=\bar{A}^{-1}\bar{B}_x u(s). \tag{4.14}$$

Similarly, the solution of $\bar{\bar{v}}_x(s)$ in (4.13) satisfies

$$\begin{aligned} \bar{\bar{v}}_x(s) &= (\bar{A}+\delta\bar{A})^{-1}\bar{B}_x u(s) \\ &= (\bar{A}+\delta\bar{A})^{-1}(\bar{A}+\delta\bar{A}-\delta\bar{A})\bar{A}^{-1}\bar{B}_x u(s) \\ &= (I-(\bar{A}+\delta\bar{A})^{-1}\delta\bar{A})\bar{A}^{-1}\bar{B}_x u(s) \\ &= (I-(\bar{A}+\delta\bar{A})^{-1}\delta\bar{A})\bar{v}_x(s). \end{aligned} \tag{4.15}$$

Therefore, the error introduced by the regularization from (4.8) to (4.13) can be described as

$$\frac{\|\bar{\bar{v}}_x-\bar{v}_x\|}{\|\bar{v}_x\|}\le\left\|(\bar{A}+\delta\bar{A})^{-1}\right\|\cdot\left\|\delta\bar{A}\right\|. \tag{4.16}$$

From the regularization criterion (4.12), we have

$$\left\|\delta\bar{A}\right\|\le tol\cdot\frac{1}{|s|}\|\bar{\Gamma}_x\|. \tag{4.17}$$

For frequency domain analysis with $s=j\omega$ in limited frequency region, we can assume

$$\frac{1}{|s|}\|\bar{\Gamma}_x\|\le\alpha\left\|\bar{A}\right\|, \tag{4.18}$$

where α is a constant. Combining (4.17) and (4.18), we have

$$\left\|\delta\bar{A}\right\|\le\alpha\cdot tol\cdot\left\|\bar{A}\right\|. \tag{4.19}$$

Substituting (4.19) into (4.16) gives

$$\frac{\|\bar{\bar{v}}_x - \bar{v}_x\|}{\|\bar{v}_x\|} \leq \left\|(\bar{A}+\delta\bar{A})^{-1}\right\| \cdot \|\delta\bar{A}\| \\ \leq \alpha \cdot tol \cdot \|\bar{A}\| \cdot \left\|(\bar{A}+\delta\bar{A})^{-1}\right\| \approx \alpha \cdot tol \cdot \kappa(\bar{A}), \tag{4.20}$$

where $\kappa(\bar{A})$ is the condition-number of the matrix $\bar{A}$. The inequality (4.20) demonstrates the controllability of the error induced by the regularization of $\bar{\Gamma}_x$. In practical applications, we can choose appropriate *tol* depending on the required accuracy.

4.4 Summary of RLCSYN

The proposed RLC circuit synthesis method RLCSYN can be outlined as follows:

Step 1. Generate the reduced order model (3.5) by SAPOR (or SPRIM) method with IOPOR technique.

Step 2. Perform the diagonalization on the $\tilde{\Gamma}_x$ in the reduced system (3.5). The consequent formulations in frequency domain are shown in (4.8).

Step 3. Choose an appropriate threshold *tol* according to the accuracy requirement and apply regularization on (4.8) to obtain the regularized system (4.13).

Step 4. Based on (4.13), synthesize equivalent circuit by unstamping procedure as described in Subsection 4.1.

The synthesized RLC circuits obtained by the proposed method have several excellent properties:

Pure RLC equivalent circuit for reduced-order models: Due to the input-output structure preserving property of IOPOR technique and block structure preserving property of SAPOR or SPRIM methods, the equivalent circuits synthesized by RLCSYN are pure RLC circuits without controlled sources.

Accurate model of the original interconnect circuit: Firstly, due to the high reduction accuracy of the MOR methods like SAPOR and SPRIM combined with IOPOR technique, the reduced system (3.5) is a close approximation of the original interconnect circuit. Secondly, in the circuit synthesis process, the error introduced by regularization can be limited in small magnitude. Therefore, the synthesized circuits preserve the input-output transfer characteristics of the original interconnect circuits with very high accuracy.

Guaranteed passivity: Firstly, since order reduction by SAPOR or SPRIM combined with IOPOR technique is based on congruent transform, thus matrices $\tilde{G}_x$, $\tilde{C}_x$ and $\tilde{\Gamma}_x$ in (3.5) are semi-positive definite. Furthermore, the diagonalization of $\tilde{\Gamma}_x$ is also based on congruent transform (4.7) and the regularization only gets rid of the smallest diagonal elements of the matrix $\bar{\Gamma}_x$. The regularized matrix $\bar{\bar{\Gamma}}_x$ as well as $\bar{C}_x$,$\bar{G}_x$ are still symmetry semi-definite. As a result, the system described by (4.13) is passive [15].

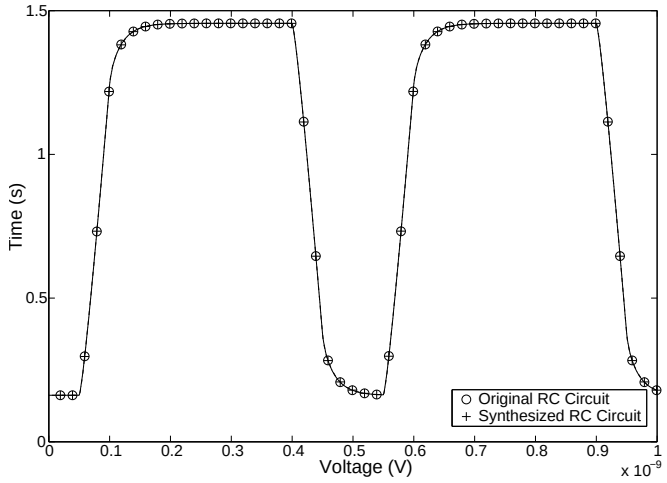

Figure 4: Comparison of transient simulation results of the original RC circuit and the synthesized RC circuit.

SPICE-simulation robustness: With the inline diagonalization and regularization techniques, the circuit synthesized by RLCSYN is robust for SPICE simulation and can be combined with analog circuits in the simulation of mixed-signal ICs.

5 Numerical results

In this section, we present numerical experiments to demonstrate the efficiency of the proposed circuit synthesis method RLCSYN. The RLCSYN prototype is implemented in MATLAB 6.5. All the experiments are conducted on a Linux workstation with Intel(R) Xeon(TM) 2.8GHz CPU and 8G RAM.

5.1 Equivalent circuit synthesis of multi-port RC circuit

The proposed RLCSYN method can be applied to multi-port RC equivalent circuit synthesis. The first example is a 16-bit bus with two shielding lines, which is modeled as an RC circuit with 3056 components. We use PRIMA [9] method and IOPOR technique to reduce this RC circuit from order 1041 to order 36. Afterwards, we synthesize an equivalent RC circuit, which has 152 components and 36 nodes, by the RLCSYN prototype. We perform SPICE transient analysis on both the original circuit and the synthesized circuit with excitations of pulse current sources at the near end of the bus lines. The voltage at the far end of the first line is considered here as the criteria for judging the accuracy. The transient simulation results are shown in Fig. 4. The transient response of the original circuit is almost the same as that of the synthesized circuit. We also perform SPICE AC analysis on both the original circuit and the synthesized circuit with current excitation at the near end of the first line. The voltage at the far end of the first line is considered as

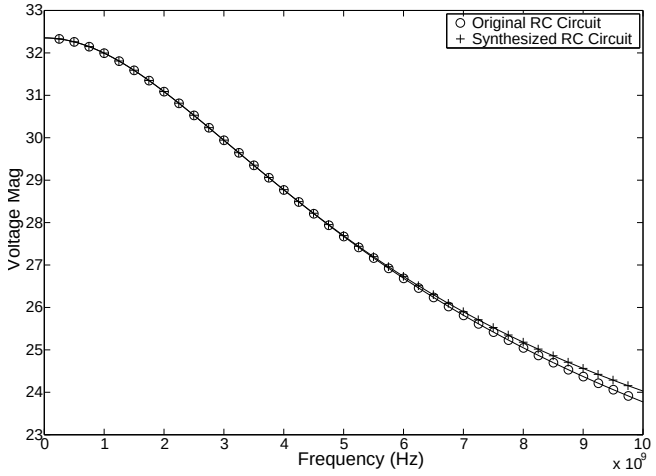

Figure 5: Comparison of AC simulation results of the original RC circuit and the synthesized RC circuit.

Table 1: Comparisons of transient and AC analysis time by SPICE.

		Original Circuit	Synthesized Circuit
RC example	Transient	1.25 s	0.05 s
	AC	25.82 s	0.34 s
RCS example	Transient	5007.59 s	90.16 s
	AC	29693.02 s	739.29 s
RLC example	Transient	2223.81 s	12.74 s
	AC	15446.72 s	90.20 s

observing point. The AC simulation results are shown in Fig. 5. The AC response of the synthesized circuit can accurately match that of the original circuit up to 5 GHz. Since no regularization is required for RC circuit, the error of AC response of the synthesized circuit in the high frequency region is due to MOR method rather than the proposed synthesis method. The transient and AC simulation time is drastically reduced for the synthesized RC circuit, as shown in Table 1.

5.2 Equivalent circuit synthesis of multi-port RCS circuit

The second example is a 64-bit bus circuit with 8 inputs and 8 outputs, which is modeled as an RLC circuit with 568300 components. The inverse of the inductance matrix of the RLC circuit is then calculated as the susceptance matrix to formulate an RCS circuit model [2]. We use SAPOR method and IOPOR technique to reduce this RCS circuit from order 16963 to order 320. Afterwards, we synthesize equivalent RLC circuits by the RLCSYN prototype. The SPICE simulation results of the original RLC circuit are taken as criteria for judging accuracy.

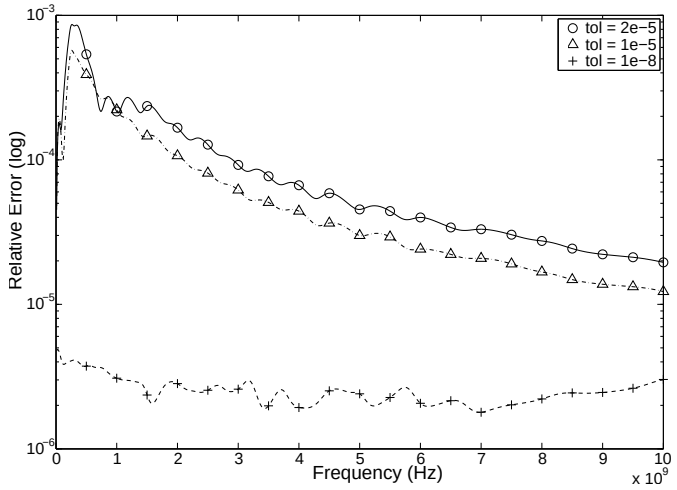

Figure 6: Error induced by regularization with different *tol* values of the RCS example.

5.2.1 Error control of regularization

If we neglect the regularization step in the synthesis procedure, the synthesized circuit encounters "internal timestep too small in transient analysis" during SPICE transient simulation. This kind of SPICE simulation breakdown attributes to the existing overlarge inductors in the synthesized circuit. In the original RLC interconnect circuit, the typical value for an inductor varies from 1 *pico henry* to 1 *micro henry*, however, the maximum inductor in the synthesized circuit reaches 30 *Mega henry*, and there are 15 inductors with value over 1 *henry*. These overlarge inductors easily cause the convergence difficulty in SPICE transient analysis.

In order to overcome the simulation difficulty caused by these overlarge inductors, we take into account the regularization in the synthesis procedure. We choose three different threshold *tol* values, i.e. 10^{-8}, 10^{-5}, 2×10^{-5}, and synthesize three different circuits, whose maximum inductors are 5×10^{-3} *henry*, 5×10^{-6} *henry* and 3×10^{-6} *henry*, respectively. Due to the elimination of overlarge inductors, SPICE transient analysis goes along smoothly for these three synthesized circuits.

We choose an output port to input port transfer function to show the errors induced by regularization. The transfer functions of the synthesized circuits are calculated and compared with those of the reduced-order models obtained by SAPOR with IOPOR technique. The relative error induced by regularization can be expressed as

$$r(s)=|\tilde{H}(s)-\bar{H}(s)|/|\tilde{H}(s)|, \tag{5.1}$$

where $\tilde{H}(s)$ denotes the transfer function of the reduced-order model obtained by SAPOR with IOPOR technique and $\bar{H}(s)$ denotes the transfer function of the synthesized circuit with regularization.

The relative errors of the three synthesized circuit with different *tol* values are shown in Fig. 6. We can see that the synthesized circuit with the smallest $tol=10^{-8}$ achieves the

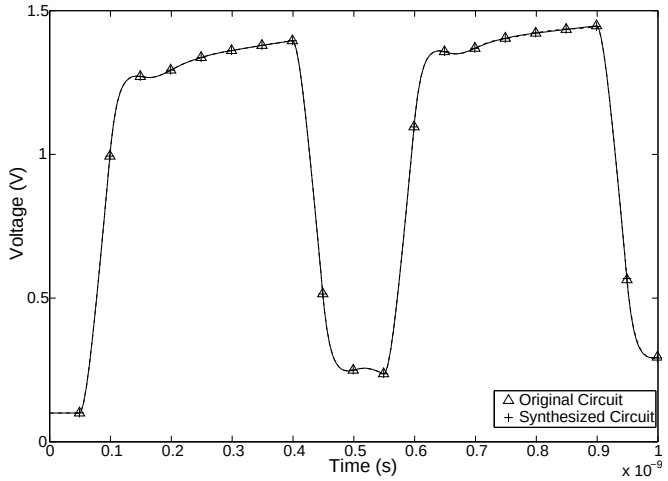

Figure 7: Comparison of transient simulation results of RCS circuit and the synthesized RLC circuit with $tol = 10^{-8}$.

highest accuracy. Furthermore, the relative error induced by regularization is below 10^{-5} when tol is chosen as 10^{-8}.

5.2.2 Transient and AC simulation results of synthesized circuit with $tol = 10^{-8}$

The synthesized RLC circuit with $tol = 10^{-8}$ has 102935 components and 320 nodes. The voltage at the far end of the first line is considered here as observing point for judging the accuracy. SPICE transient analysis are performed on both the original RLC circuit and the synthesized circuit with excitations of pulse current sources at eight inputs. The transient simulation results are shown in Fig. 7. The transient response of the synthesized circuit is indistinguishable from that of the original RLC circuit. We also perform SPICE AC analysis on both the original RLC circuit and the synthesized RLC circuit with current excitation at the near end of the first line. The voltage at the far end of the first line is considered as observing point. The AC simulation results are shown in Fig. 8. The low frequency response and DC characteristic of the synthesized circuit matches those of the original circuit well. Since the error of the transfer function induced by regularization is below 10^{-5} when tol is chosen as 10^{-8}, the error of the AC response of the synthesized circuit in high frequency region attributes to MOR method rather than the proposed synthesis method. The transient and AC analysis time by SPICE is also given in Table 1. Up to 50x speedup of transient and AC simulations is achieved.

5.3 Equivalent circuit synthesis of multi-port RLC circuit

The third example is a 64-bit bus circuit with 8 inputs and 8 outputs, which is modeled as an RLC circuit with 285292 components. We use SPRIM method with IOPOR technique to reduce this RLC circuit from order 8514 to order 160. Afterwards, we conduct similar

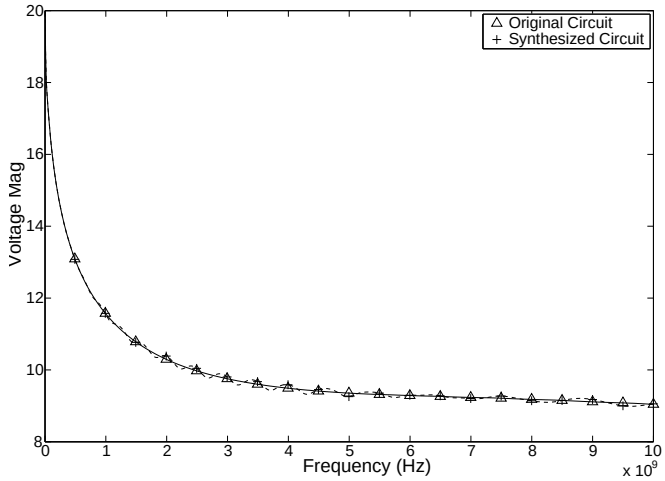

Figure 8: Comparison of AC simulation results of RCS circuit and the synthesized RLC circuit with $tol = 10^{-8}$.

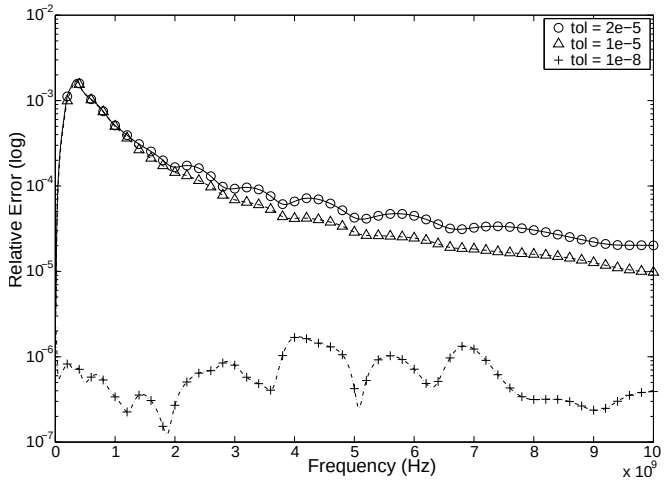

Figure 9: Error induced by diagonalization and regularization with different tol values of the RLC example.

experiments as the RCS example by the RLCSYN prototype. Similar results are derived as shown in Figs. 9, 10 and 11. It can be seen from Fig. 9 that the relative error induced by regularization is below 10^{-5} when tol is chosen as 10^{-8}. In Fig. 10, the transient response of the synthesized circuit matches that of the original circuit well. In Fig. 11, the low frequency response and DC characteristic of the synthesized circuit match those of the original circuit well. The error of the AC response of the synthesized circuit in high frequency region is due to MOR method rather than the proposed synthesis method, since the error of the transfer function induced by regularization is below 10^{-5} when tol is chosen as 10^{-8}. Moreover, up to 185x speedup of transient and AC simulations is achieved as shown in Table 1.

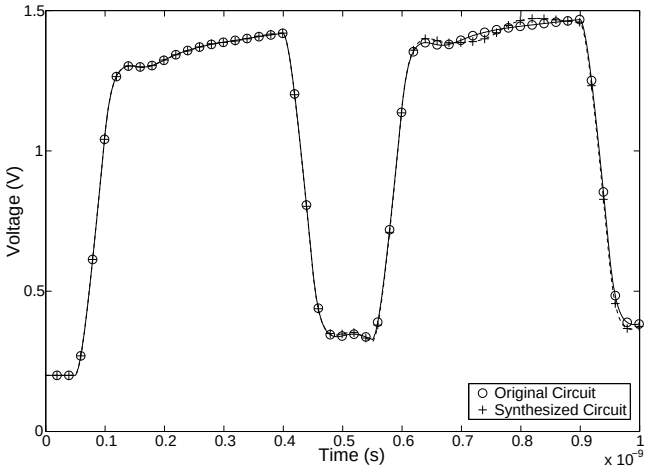

Figure 10: Comparison of transient simulation results of RLC circuit and the synthesized RLC circuit with $tol=10^{-8}$.

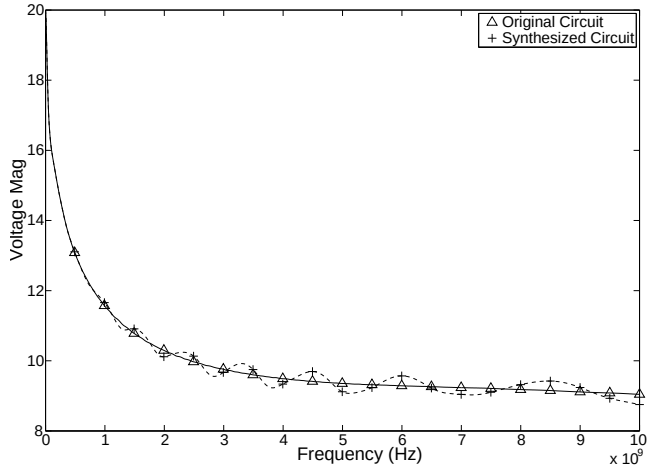

Figure 11: Comparison of AC simulation results of RLC circuit and the synthesized RLC circuit with $tol=10^{-8}$.

6 Conclusion

This paper proposes an RLC circuit synthesis method RLCSYN for reduced-order models of interconnect circuits obtained by Krylov subspace based MOR methods. IOPOR technique is proposed to preserve the input and output structures in the reduced-order systems. Inline diagonalization and regularization techniques are proposed to enhance the robustness of inductance synthesis. The synthesized circuit has the following pleasant merits such as pure RLC equivalent circuit, passivity preserving, accurate modeling of the original interconnect circuit and SPICE-simulation robustness, which makes the proposed method very promising in practical applications of interconnect analysis and modeling.

Acknowledgments

This research is supported partly by NSFC research project 90307017 and 60676018, partly by the National Basic Research Program of China under the grant 2005CB321701, partly by Cross-Century Outstanding Scholar's fund of Ministry of Education of China, partly by the doctoral program foundation of Ministry of Education of China 20050246082, partly by Shanghai Dawn Project 200601, partly by the National Science Foundation (NSF) under Grant CCR-0306298.

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