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RLC Equivalent Circuit Synthesis Method for Structure-Preserved Reduced-Order Model of Interconnect in VLSI

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Abstract. This paper aims to explore RLC equivalent circuit synthesis method for reduced-order models of interconnect circuits obtained by Krylov subspace based model order reduction (MOR) methods. To guarantee pure RLC equivalent circuits can be synthesized, both the structures of input and output incidence matrices and the block structure of the circuit matrices should be preserved in the reduced-order models. Block structure preserving MOR methods have been well established. In this paper, we propose an embeddable *I*nput-*O*utput structure *P*reserving *O*rder *R*eduction (IOPOR) technique to further preserve the structures of input and output incidence matrices. By combining block structure preserving MOR methods and IOPOR technique, we develop an RLC equivalent circuit synthesis method *RLCSYN* (RLC SYNthesis). Inline diagonalization and regularization techniques are specifically proposed to enhance the robustness of inductance synthesis. The pure RLC model, high modeling accuracy, passivity guaranteed property and SPICE simulation robustness make *RLCSYN* more applicable in interconnect analysis, either for digital IC design or mixed signal IC simulation.

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1 Introduction

In modern high-speed nano-scale ULSI design, interconnects have become a dominant factor in determining the performance of the whole chip. However, the extracted interconnect circuits, either based on RLC or RCS model, turn out to be extremely large, which poses great challenges to interconnect analysis techniques [1, 2].

Model order reduction (MOR) has become the state-of-the-art technique for fast simulation of the interconnect circuits with large dimensions. Recently, RLC-in-RLC-out MOR has become a research intensive area [3–7]. In a typical design flow, all kinds of circuit analysis and verification procedures, such as static timing analysis, dynamic simulation, noise analysis, circuit checking and power analysis, take extracted RLC circuits as inputs. If RLC equivalent circuit of the reduced-order models is not available, all the downstream circuit simulators and associated programs have to be modified to handle transfer functions or state-space models of interconnects [8]. RLC equivalent circuit also plays an important role in mixed signal IC simulation, where linear and nonlinear circuits need to be simulated together. Moreover, some analysis tools such as circuit checker only accept RLC circuits as inputs [3].

Realizable reduction methods providing RLC-in-RLC-out (RC-in-RC-out) reduction schemes are proposed in [3–5]. Since these reduction methods are based on selectively removing non-terminal nodes by Guassian elimination, the applications of these methods would be limited. In [3, 5], only the nodes satisfying strict nodal time constant constraints can be eliminated. These constraints would limit the circuit reduction ratio, which makes [3, 5] serve as a preprocessing step before feeding extracted circuits to moment-matching based MOR methods [3]. In [4], although high reduction ratio is achievable, high order approximation of admittances induced by elimination should be calculated and substituted in each elimination to guarantee accuracy of the reduced-order circuit model, which would be computation intensive.

Krylov subspace based MOR methods are the state-of-the-art techniques for interconnect analysis. Compared with realizable reduction methods, Krylov subspace based MOR methods can achieve higher reduction ratio and accuracy [9]. However, RLC equivalent circuit synthesis method for Krylov subspace based MOR methods has not been well established. In [10], Freund et al. proposed an equivalent RC circuit synthesis method for single-port RC reduced-order models derived from SyPVL method. Equivalent circuit synthesis techniques for reduced-order models of multi-port RLC circuits obtained by PRIMA(-like) algorithm(s) are well investigated in [7]. However, since the input-output and block structures are not preserved in PRIMA(-like) algorithm(s), controlled sources should be introduced in the synthesized circuits in these methods. Up to now, pure RLC equivalent circuits are not achievable yet.

In this paper, we propose an RLC equivalent circuit synthesis method for reduced-order model obtained by Krylov subspace based MOR methods. For the synthesis of pure RLC models, both the structures of input and output incidence matrices and the block structures of the circuit matrices should be preserved. We employ SPRIM [11] or